

# PDSOI and Radiation Effects: An Overview

Joshua B. Forgione, NASA GSFC / George Washington University

## ABSTRACT

Bulk silicon substrates are a common characteristic of nearly all commercial, Complementary Metal-Oxide-Semiconductor (CMOS), integrated circuits. These devices operate well on Earth, but are not so well received in the space environment. An alternative to bulk CMOS is the Silicon-On-Insulator (SOI), in which a dielectric isolates the device layer from the substrate. SOI behavior in the space environment has certain inherent advantages over bulk; a primary factor in its long-time appeal to space-flight IC designers.

The discussion will investigate the behavior of the Partially-Depleted SOI (PDSOI) device with respect to some of the more common space radiation effects: Total Ionized Dose (TID), Single-Event Upsets (SEUs), and Single-Event Latchup (SEL). Test and simulation results from the literature, bulk and epitaxial comparisons facilitate reinforcement of PDSOI radiation characteristics.

## 1.0 Introduction

A ubiquitous element of today's integrated circuits is the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET). Complementary MOS (CMOS) circuits make use of both MOSFET types: N-channel MOS (NMOS) and P-channel MOS (PMOS). CMOS is almost single-handedly responsible for the rapid acceleration of personal computer power in line with Moore's famous law.

It is not well known, outside the science and engineering community, that one cannot place a personal computer in the space environment and expect it to function for long. One of the main reasons for the rapid degradation of commercial electronics outside the Earth's atmosphere is the natural space radiation environment. Aside from man-made radiation found in nuclear power and weapons application, very little high-energy radiation impinges on terrestrial electronics; explaining why people rarely consider radiation when purchasing their home computer.

There are many ways in which radiation can damage electronics. Three are the discussion's focus: Total Ionizing Dose (TID), Single Event Upsets (SEU) and Single-Event-Latch-up (SEL). All involve the penetration of highly charged particles into sensitive regions of an integrated circuit. Other Single-Event Effects (SEE), such as Analog and Digital Single-Event Transients (ASET's, and DSET's, respectively), are covered in brief.

Once upon a time, the aerospace industry was the driver of both space-flight and commercial electronics development. The decline in government-funded space endeavors and the personal computer boom has had its impact on development of space-qualified electronics. As a result, many integrated circuits whose designs date back to the 70's and 80's still find heavy use on spaceflight designs. To utilize functionality found on commercial, terrestrial integrated circuits (ICs), spaceflight programs often fund

development of Application Specific Integrated Circuits (ASICs). These custom ICs are expensive, but yield the low power and radiation tolerance needed to get the job done. Over the past 40 years, many military and aerospace ASICs have been built utilizing Silicon-On-Insulator (SOI) technology<sup>[1]</sup>.

Recently, the commercial electronics industry invested heavily to understand the behavior of the SOI MOSFET, due to its inherent high-frequency and low-power characteristics<sup>[2]</sup>. The commercial investment in SOI meant the radiation-effects understanding of SOI refined, to the benefit of the space-flight design community.

The fundamental reasons for the rise of CMOS fabricated on a bulk substrate are due to availability of materials and processing techniques<sup>[2]</sup>. At the time CMOS rose in popularity, device deposition onto an insulator, hence separating device and substrate, was simply not feasible. In the past twenty years, process techniques advanced, the SOI concept has been revisited, and the technology gained enough steam to progress from obscure to nearly mainstream. With CMOS underpinning the vast majority of today's circuits, it is not surprising the MOSFET is the most common implementation of Silicon-On-Insulator technology.

Typical CMOS is fabricated on a "bulk" substrate. In the device of Figure 1b, the n-channel device structure on the left incorporates the substrate. The p-channel device on the right of Figure 1b is formed by diffusing an n-well into the p-substrate. In an SOI device (Figure 1a), a thick, insulating, SiO<sub>2</sub> layer isolates adjacent devices from each other and the substrate. This conceptually simple rearrangement yields significant behavioral changes. For terrestrial and space-borne electronics, particular implementations of SOI can result in lower power, faster switching, and improved radiation performance<sup>[2]</sup>. The focus of this discussion is on the latter of the three: how the Partially-Depleted SOI CMOS device behaves with respect to common space radiation effects.



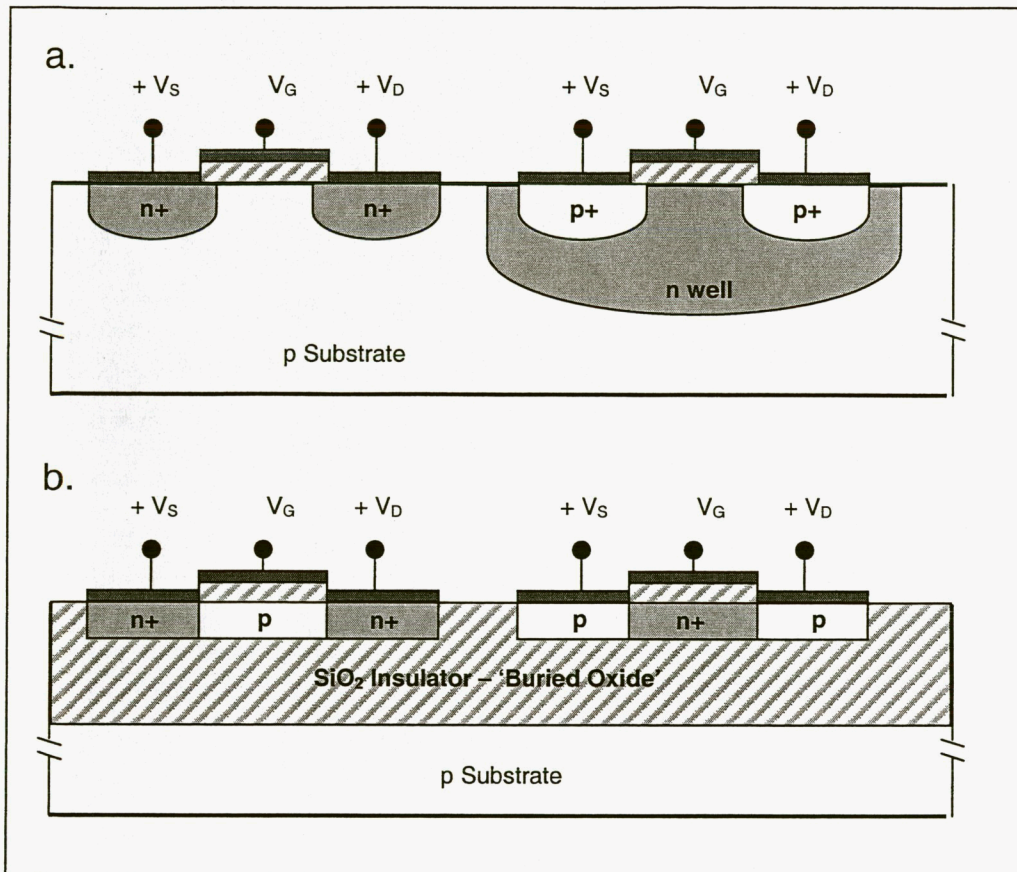


Figure 1: Bulk (a) and SOI (b) CMOS comparison.

## 2.0 The SOI MOSFET

### 2.1 Overview

The basic operation of the bulk MOSFET is well documented<sup>[3,4]</sup>. Although SOI has risen in popularity, it is still considered a specialty area, and a demonstration of its basic behavior warrants discussion. The following discussions assume an n-channel, enhancement device, unless otherwise noted. By default, equations will represent long-channel approximations for simplicity.

### 2.2 Silicon-On-Insulator Types

Two primary SOI implementations exist. The difference between partially depleted (PD, PDSOI) and fully-depleted (FD, FDSOI) lies in the thickness,  $t_{si}$ , of the silicon device layer. The device-layer thickness dictates the degree to which the silicon

under the gate can deplete. The bulk-device, depletion-region width,  $x_d$ , maximizes at channel inversion onset, and

$$x_d = x_{dmax} = \sqrt{\frac{2\epsilon_s |\Phi_p|}{N_a}}, \quad (1)$$

where  $\Phi_p$  is the charge-neutral body potential, given by

$$\Phi_p = \frac{kT}{q} \ln \left( \frac{N_a}{n_i} \right) \quad (2)$$

In a partially-depleted device (Figure 2a), the device-layer width is  $t_{si} > 2x_{dmax}$ , and applied gate voltage can never deplete the entire channel. In contrast, the fully-depleted device (Figure 2b) has  $t_{si} < 2x_{dmax}$ , and an applied gate bias can deplete the entire device layer.

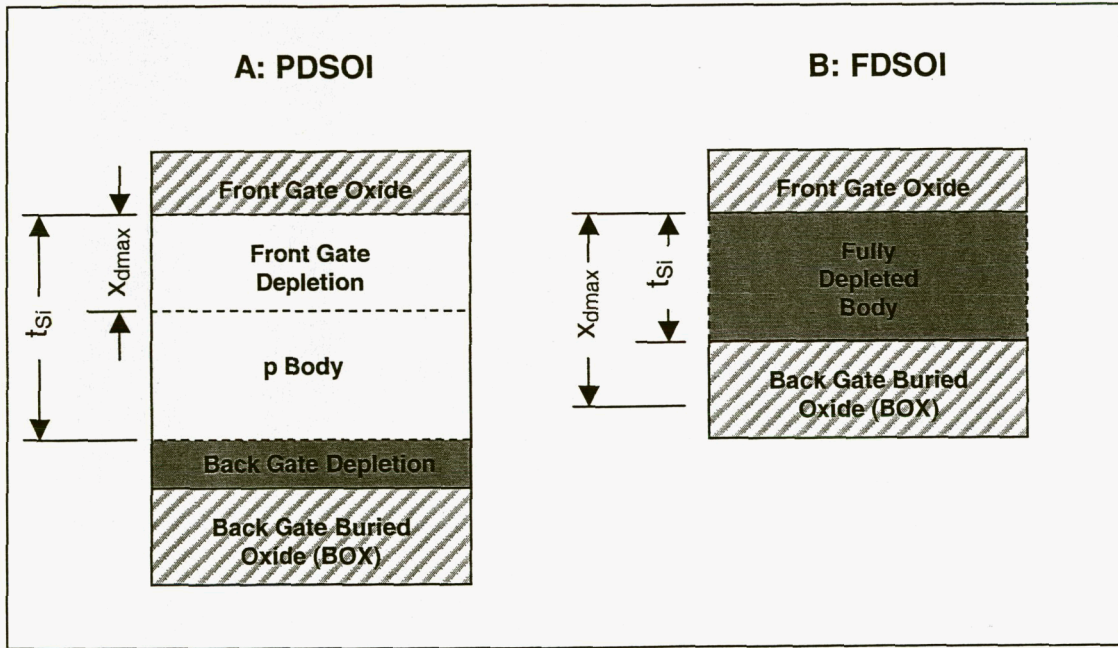


Figure 2: In the PDSOI device (a), the front and back-gate depletion regions never interact, as in the FDSOI device (b).

The difference determinant between the SOI implementations is evident when one observes the FDSOI overlap of front-and-back gate depletion regions (Figure 2b). The front and back regions can each accumulate, deplete, or invert, resulting in nine possible FDSOI modes of operation. The lack of contact between the front and back depletion regions is a major factor in PDSOI behavior as compared to bulk. The buried oxide isolates the body from the substrate, and a neutral, floating body is possible in PDSOI. When the body is terminated, the basic PDSOI characteristics mirror bulk. However, perfect body termination is often unrealizable; hence the 'floating body effect' is the major influence on PDSOI device behavior.

To date, PDSOI has been most widely embraced by commercial manufacturers. Due to the sophistication required of FDSOI wafer fabrication, the first commercial manufacture of FDSOI devices did not occur until 2002<sup>[5]</sup>. In general, the FDSOI device



is also more complex to analyze than PDSOI. Conveyance of the fundamental principles of radiation response in SOI compare to bulk is more clearly achieved using the PDSOI model, and as such, the n-channel, enhancement-mode, PDSOI device forms the basis of comparison for the remainder of the discussion.

## 2.3 Floating-Body Effects in PDSOI

### 2.3.1 Overview

The front-and-back depletion regions of the PDSOI device sandwich a neutral, silicon, body region. When the body is tied to a reference potential, PDSOI behavior mirrors bulk, and is classically expressed as<sup>[3],[4]</sup>

$$V_{th} = V_{FB} + 2|\Phi_p| - \frac{Q_d}{C_{ox}} \quad (3)$$

and

$$Q_d = -qN_a x_d \quad (4)$$

where  $V_{FB}$  is the flat-band voltage, and  $C_{ox}$  the oxide capacitance.  $Q_d$  is the depletion-layer charge; negative in the case of an n-channel device.

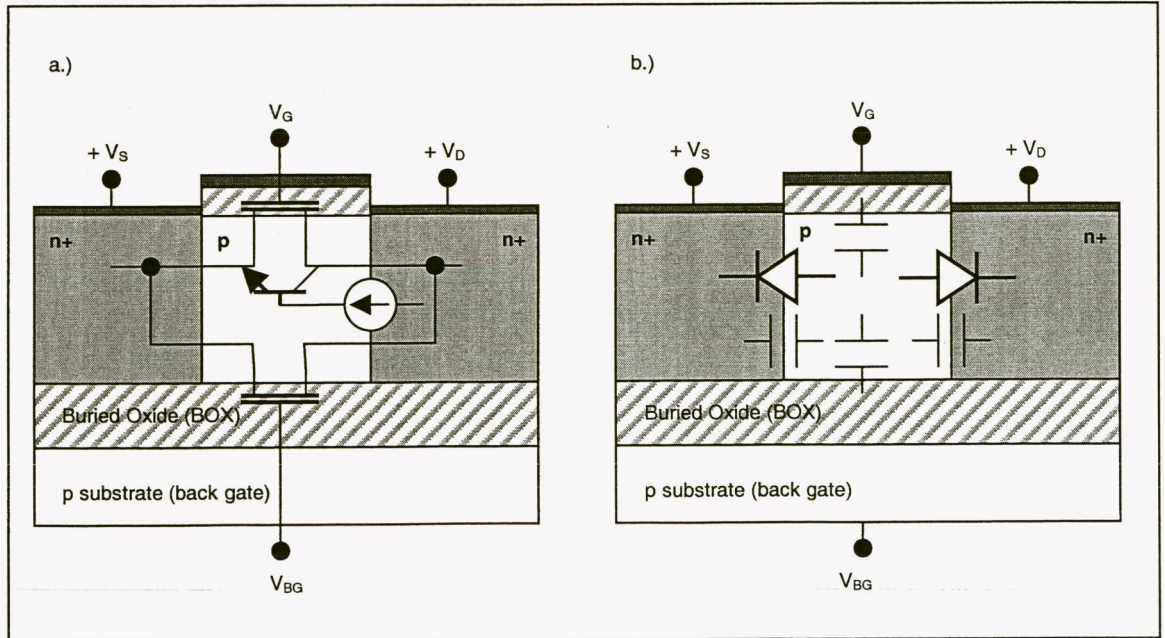


Figure 3: Transistors (a), capacitors, and diodes (b) embedded in the PDSOI MOSFET structure.

Unfortunately, the practical implementation of body ties is not a trivial matter. The un-terminated body charge can vary over time with applied terminal voltages. Charge flows into the body via two mechanisms: impact ionization current near the drain junction (represented by the current source in Figure 3a), and leakage current across the

reverse-biased drain-body and source-body diodes (Figure 3b). Both of these mechanisms cause the body to accumulate charge, and vary in potential. Two means exist for the body to relinquish its charge. Over time, enough charge accumulates in the body to forward bias one of the junction diodes, and the body passes current to either the source or drain. Second, a source or drain voltage rise capacitively couples to the body; the body-potential rise may forward-bias one of the junctions and also pass current through the device<sup>[6]</sup>.

Body-bias variance affects the threshold voltage and current drive of the device. With the source used as a reference potential, equations (3) and (4) can be rewritten to include the influence of drain ( $V_D$ ) and body ( $V_B$ ) potentials<sup>[4]</sup> in a device:

$$V_{th} = V_{FB} + V_D + 2|\Phi_p| - \frac{Q_d}{C_{ox}} \quad (5)$$

$$Q_d = -\sqrt{(2\epsilon_s q N_a (2|\Phi_p| + V_D - V_B))} \quad (6)$$

A typical dependence of threshold voltage on body potential is shown in the dotted line of Figure 4. In typical SOI applications,  $V_B > 0$ ; the converse is typical for bulk<sup>[7]</sup>.

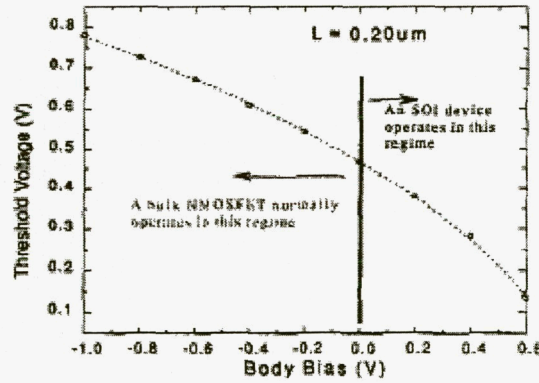


Figure 4: Body Bias ( $V_B$ ) vs. Threshold Voltage ( $V_{th}$ )<sup>[7]</sup>

An increase in body-potential for the n-channel device lowers the threshold voltage, resulting in an increase in drain current<sup>[4]</sup>:

$$I_D = k \left[ \left( V_G - V_{Th} - \frac{1}{2} V_D \right) V_D \right] \quad (7)$$

where  $k = \mu_n C_{ox} \frac{W}{L}$ , and  $V_G$  the gate voltage.

## 2.4 Impact Ionization and the BJT Effect

### 2.4.1 Impact-Ionization Mechanisms

Impact ionization is a purely generative process in semiconductors that occurs when a high electric field ( $\vec{E}$ ) and current density ( $\vec{J}$ ) run concurrently in a device. The recombination rate,  $R$ , in a device due to impact ionization can be expressed as



$$R^{II} = -(G_n^{II} + G_p^{II}), \quad (8)$$

where negative R indicates net generation.  $G_n^{II}$  and  $G_p^{II}$  are the electron-and-hole impact-ionization generation rates, respectively, and defined as

$$G_p^{II} = \alpha_p \frac{|\overline{J_p}|}{q} = \left[ \alpha_p^\infty e^{\left\{ -\left( \frac{E_p^{crit}}{|\overline{E}|} \right)^{\beta_p} \right\}} \right] \bullet \frac{|\overline{J_p}|}{q} \quad (9)$$

$$G_n^{II} = \alpha_n \frac{|\overline{J_n}|}{q} = \left[ \alpha_n^\infty e^{\left\{ -\left( \frac{E_n^{crit}}{|\overline{E}|} \right)^{\beta_n} \right\}} \right] \bullet \frac{|\overline{J_n}|}{q} \quad (10)$$

Equations (9) and (10) can be boiled down to their pertinence by ignoring the constants  $\alpha$  and  $\beta$ , and empirical expression  $E^{crit}$ , and instead qualitatively observing generation is a maximum when the field and current are high and in the same direction. In a MOSFET, this scenario occurs near the reverse-biased, drain depletion region, where the channel current ( $I_{ch}$ ) runs in the same direction as a high electric field caused by  $V_{DB}$ . Under the influence of the drain electric field, the generated electrons and holes sweep into the drain and body, respectively. This mechanism is equivalent to a current source ( $I_{body}^{II}$ ) from drain to body, as shown in Figure 3a.

For bulk devices, impact ionization results in device wear-out over time. Several, more interesting, effects occur in the PDSOI device. The influx of body current increases the floating-body potential and causes fluctuations in the threshold voltage,  $V_{th}$ . In the sub-threshold region ( $V_G < V_{th}$ ), the weak-inversion drain current is still large enough to cause impact ionization at the drain. The subsequent decrease in the threshold voltage causes the  $I_D(V_G)$  curve to shift to the left, and the slope of the sub-threshold current can increase up to 60mV/decade<sup>[2]</sup>. These unwanted effects are further compounded by a bipolar-junction transistor (BJT) structure inherent in the device (Figure 3a).

#### 2.4.2 BJT Effects

The n-channel, SOI MOSFET source, floating-body, and drain act as BJT emitter, base, and collector of a BJT, respectively. The BJT amplifies the body current by its gain factor  $\beta_f$ , resulting in a drain-current increase

$$\Delta I_D = \beta_f I_{body} = \beta_f I_{body}^{II}. \quad (11)$$

Given high minority carrier lifetimes and significant drain voltage, the BJT can induce a positive-feedback loop that creates an infinite sub-threshold slope and hysteretic behavior in the device  $I_D(V_G)$  curve. If  $V_D$  is large enough, the positive-feedback loses its hysteretic behavior, disallows device turn-off, leading to device latch-up, as shown in Figure 5<sup>[2]</sup>. Body ties to a reference potential allow the generated holes a path to leave the device, and eliminate this unwanted effect.

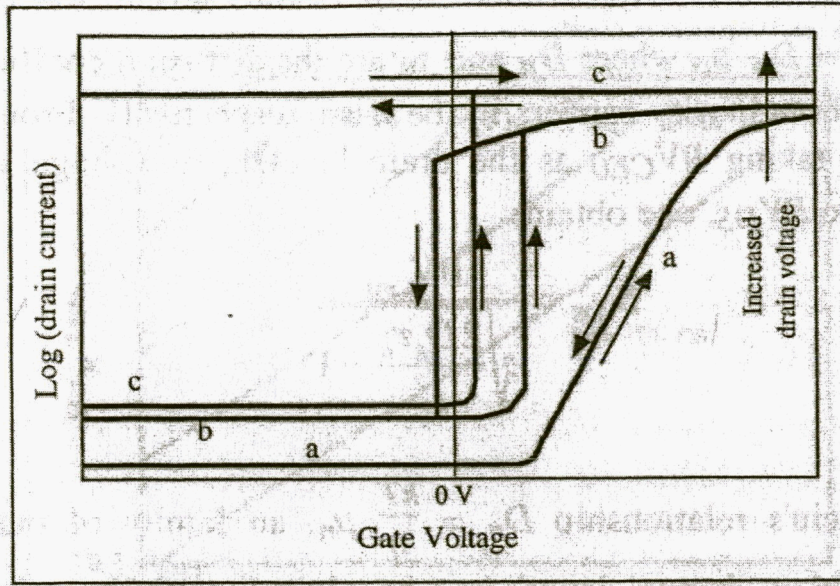


Figure 5: Illustration of the single-transistor latch. "Normal" sub-threshold slope at low drain voltage (a), infinite sub-threshold slope and hysteresis (b) and device "latch-up" (c)<sup>[2]</sup>.

### 2.4.3 Body Ties

It seems the entire floating-body characteristic of the PDSOI MOSFET is a real nuisance. Nullification of the floating-body effects means assets of SOI can be achieved with the same device behavior as bulk. It appears much more sensible to tie the body to a known reference potential and forget about the floating-body effects.

All of these statements are true. If the body is tied to a ground reference, the charge associated with the floating body has an escape path, and the characteristics of the PDSOI transistor mirror those of bulk. However, the practical reality is not quite so simple. When one takes a device-level perspective, the issue becomes clear. Creation of an individual, low-resistance, body tie for each transistor consumes significant space in the device. From the typical example shown in Figure 4, one can see the resistance, and hence, potential, vary for each transistor body due to the varied distances to the shared contact. Figure 7 shows the bipolar gain  $\beta_f$  as a function of distance from the body contact<sup>[1]</sup>. The end result is not every MOSFET's BJT can fully disable; some are still able to turn on and amplify  $I_{body}$ . Therefore, arrangement of the body contacts within a PDSOI device is crucial to suppressing the BJT effect.



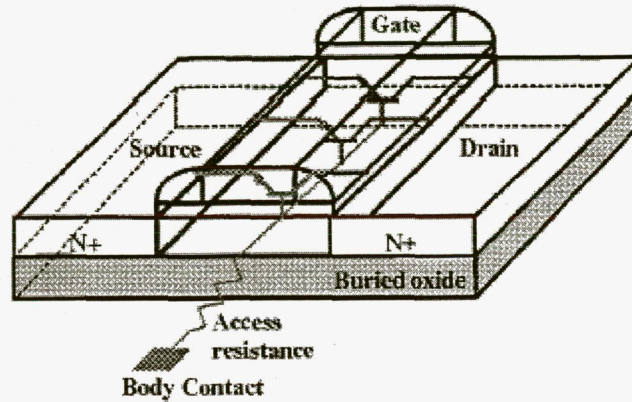


Figure 6: 3D representation of a NMOS/SOI transistor with external body contact (BC), showing the parasitic BJT connecting source and drain<sup>[8]</sup>

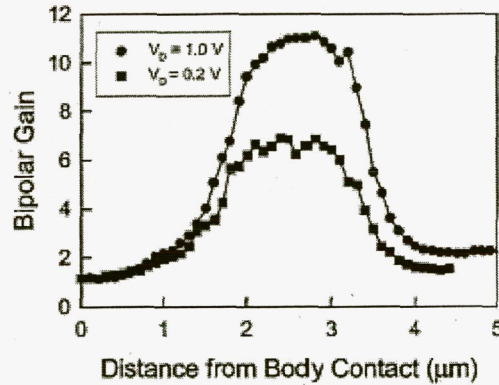


Figure 7: Variation of  $\beta_f$  as a function of body contact distance<sup>[1][8]</sup>

Sophisticated techniques exist for terminating the body, and radiation-hard devices have been created using these approaches. However, the problem persists as device size decreases, and more novel approaches for device geometries are required.

#### 2.4.4 The Back-Side Device: A Second MOSFET

A close look at the SOI MOSFET structure reveals not one, but two MOS devices. The back-channel device utilizes the BOX as a gate oxide, substrate as a back gate, and device-layer Si/BOX interface as a channel. The applied back-gate voltage can cause accumulate, deplete, or invert the back channel, as in any MOS structure. Since the source and drain permeate through the entire device layer, the inverted channel permits an undesired leakage current in the device. Significant leakage current can shift the primary device's threshold voltage to the point of failure. Deep back-side doping and substrate grounding raise the threshold voltage of the back-side device, and minimize its deleterious effects<sup>[6]</sup>.

The fundamental, characteristic differences between PDSOI devices and their bulk cousins are due to the un-terminated body in PDSOI transistors. The floating body

effects lead to threshold and drain current fluctuations, and a parasitic BJT with the potential to seriously damage the device. The floating body effects can be alleviated using body contacts. Additionally, an embedded, second MOS structure can produce unwanted effects in the SOI device. The radiation environment aggravates the PDSOI's weak points, and though complex, body ties and back-gate adjustments become absolutely necessary. The basic radiation mechanisms will find context via the subsequent discussion of the space radiation environment.

## 3.0 The Space Radiation Environment

### 3.1 Informal definition of the space radiation environment

The word radiation often carries a loosely-defined, science-fiction inspired, connotation. Radiation is some sophisticated, invisible energy blasted from futuristic cannons between groups of futuristic humans and antagonist aliens, all brought to life by low-tech, 1950s, sci-fi 'B' movies. The fact is one can conceive radiation as something simple and base; radiation means concentrations of highly-energetic particles. On Earth, electronic devices experience radiation primarily via man-made forms; nuclear weapons and power plants are two common examples.

An electronic device onboard a spacecraft ascends from the Earth's surface, departs from the planet's terrestrial environment, and enters another: the space radiation environment. The Earth's environments depend on a slew of factors, and are highly variable; space's environments are no exception. Concentrations and types of particles presented to a device in orbit depend primarily on spacecraft altitude and angle of inclination, solar activity, and spacecraft shielding<sup>[9]</sup>.

Further, two primary sources of particles are of interest in studying device radiation response. Cosmic rays, both of solar and galactic origin, bring particles from outside the Earth's atmosphere. Heavy ions and highly-energetic protons typically comprise cosmic rays. Protons, electrons, and some heavy ions trapped inside the Earth's magnetic field constitute the second type of space radiation experienced by space-flight electronics.

## 3.2 Sources and Distribution of Radiation

### 3.2.1 Cosmic Rays: Galactic and Solar

Galactic Cosmic Rays (GCR) originate outside of the solar system, and form an ever-present background radiation. This background is comprised of 87 percent protons, 12 percent He nuclei, and 1 percent heavier ions<sup>[10]</sup>. This composition can be deceiving. When one considers Single Event Effects (SEE), heavy ions often deposit more energy per path-length than protons.

The total radiation due to cosmic rays experienced by a device in space is the sum of the background GCR, and the variable solar cosmic rays. Not surprisingly, solar cosmic rays vary with solar activity. The solar cycle is, on average, 22 years long, with



peaks in activity every 11 years. Solar flares are random events, adding energetic protons (90-95%), alpha particles, and heavy ions to the GCR. Solar flares typically reach Earth within 10 minutes of emission, peak in two hours to one day, and die out within a week.

### 3.2.2 The Magnetosphere

The magnetosphere is a volumetric magnetic field surrounding Earth. The magnetosphere both traps and dictates particle motion within the field. These particle concentrations move both spirally between the Earth's poles, and in an east-west (electrons and protons, respectively) drift. Over time, particle motion creates zones of motion referred to as the Van Allen Belts. Two zones comprise the Van Allen Belts; an inner zone and an outer zone.

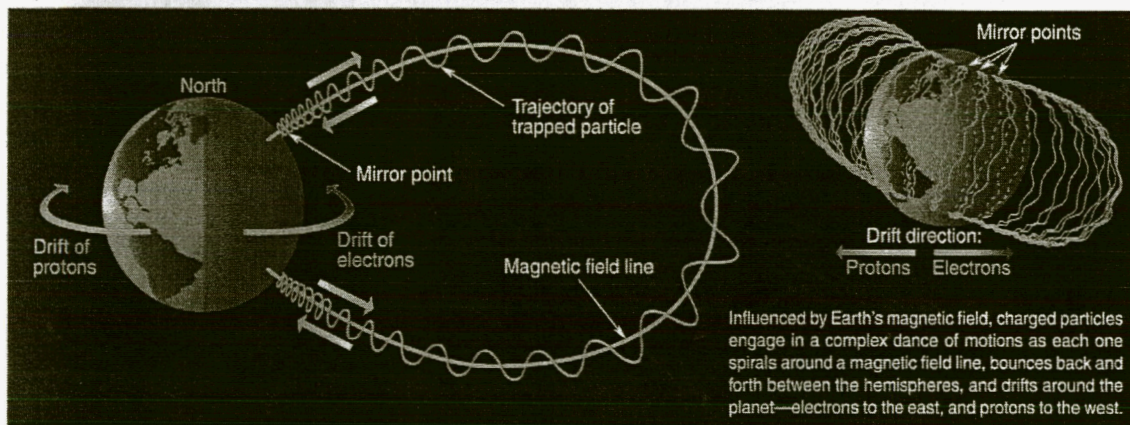


Figure 8: Particle motion in the magnetosphere<sup>[10]</sup>

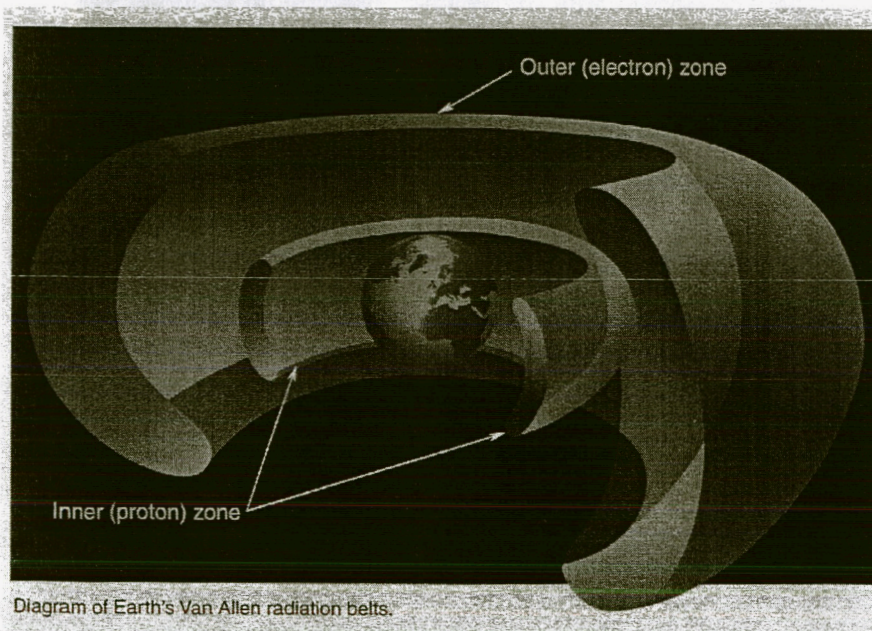


Diagram of Earth's Van Allen radiation belts.

Figure 9: Diagram of Earth's Van Allen radiation belts<sup>[10]</sup>



In the inner zone, GCR collisions with atmospheric atoms produce secondary neutrons. These neutrons tend to decay to inner-zone protons, with intensity peaks at roughly 3000 km above Earth's surface. The GCR's slow time variance and its relatively long particle lifetimes give the inner zone a fairly stable characterization. However, the inner belt has one variation of significant importance. The South Atlantic Anomaly (SAA) is the result of an imperfection in the Earth's geomagnetic sphere above the South Atlantic Ocean. In Low-Earth Orbit (LEO), proton-flux-increases of up to four orders of magnitude, with energies greater than 30 MeV, exist in the SAA as compared to other regions of the Earth. Radiation effects associated with high-energy particles, such as SEE, dramatically increase in occurrence over the SAA.

The outer zone is more volatile. Particle interactions from solar activity and interplanetary magnetic fields, both sources of a highly variable nature, characterize the outer zone. The more volatile zone consequently has shorter trapped-particle lifetimes and the highest energies of trapped electrons. Electrons in the outer Van Allen Belts reach energies up to 7 MeV<sup>[11]</sup> with peak intensities in the 12,000 to 22,000 km altitude range<sup>[10]</sup>.

One could argue, at the most base level, electronic devices are simply man-made structures, composed of carefully selected and processed materials, with the sole purpose of moving charge in specific directions, at specific rates. To the degree of fabrication precision, IC designs are intricate, careful, and deliberate; charge is intended to operate in a very particular way. When bombarded with heavily energetic particles of a quasi-random nature, the result is not surprising: the impinging charges make the device work in a way in which it was not intended. Some effects cause the device to slowly degrade over time, and some result in immediate failure. Other effects are 'soft,' since they do not result in permanent failure, proper operation can be restored. A chart of radiation effects for various orbits is shown in Figure 10.

Space hazard	Spacecraft charging		Single-event effects			Total radiation dose		Surface degradation		Plasma interference with communications	
Specific cause	Surface	Internal	Cosmic rays	Trapped radiation	Solar particle	Trapped radiation	Solar particle	Ion sputtering	O <sup>+</sup> erosion	Scintillation	Wave refraction
LEO <60°											
LEO >60°											
MEO											
GPS											
GTO											
GEO											
HEO											
Inter-planetary											

Important
  Relevant
  Not applicable

Space environment hazards for typical orbits. Key: LEO <60°—low Earth orbit, less than 60 degrees inclination; LEO >60°—low Earth orbit, more than 60 degrees inclination; MEO—medium Earth orbit; GPS—Global Positioning System satellite orbit; GTO—geosynchronous transfer orbit; GEO—geosynchronous orbit; HEO—highly elliptical orbit; O<sup>+</sup>—atomic oxygen.

Figure 10: Radiation effects for various orbits<sup>[10]</sup>



## 4.0 SOI and Radiation Effects

### 4.1 SOI and Single-Event Effects (SEE)

#### 4.1.1 SOI and Single-Event Latchup (SEL)

One of the most severe effects of radiation on CMOS devices is CMOS latch-up. Examination of the fundamental bulk device structure shown in Figure 1a may lead one to question if the lack of isolation between adjacent devices has any impact on operation. A closer look reveals the basic CMOS device structure creates two parasitic transistor elements, shown in Figure 11. These parasitic elements form an interconnected npn and pnp bipolar transistor structure, or thyristor, in the device (Figure 12). Thyristors are feedback devices commonly used to switch large currents<sup>[12]</sup>, but in the CMOS device, they are a nascent time-bomb.

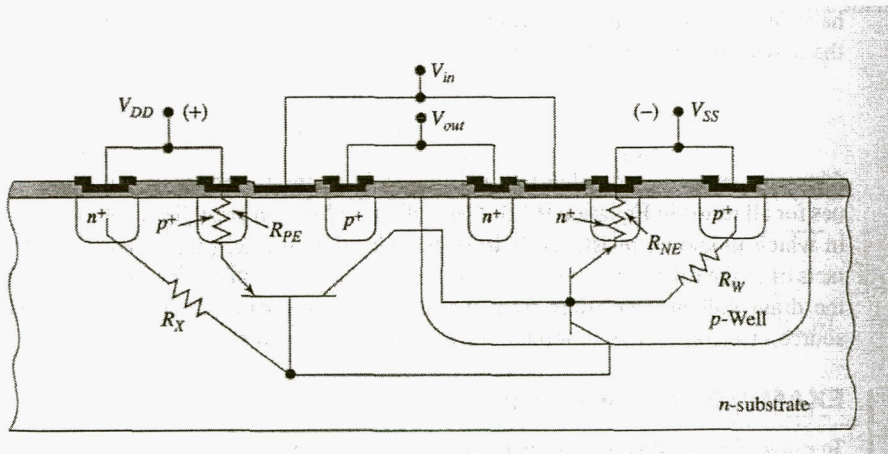


Figure 11: Cross section of a p-well CMOS inverter, with parasitic elements pertinent to latch-up<sup>[3]</sup>

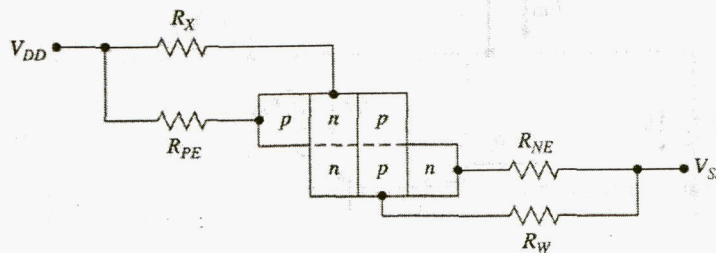


Figure 12: Circuit and schematic representation of the thyristor, created via cross-coupled, parasitic npn and pnp transistors in p-well CMOS<sup>[3]</sup>

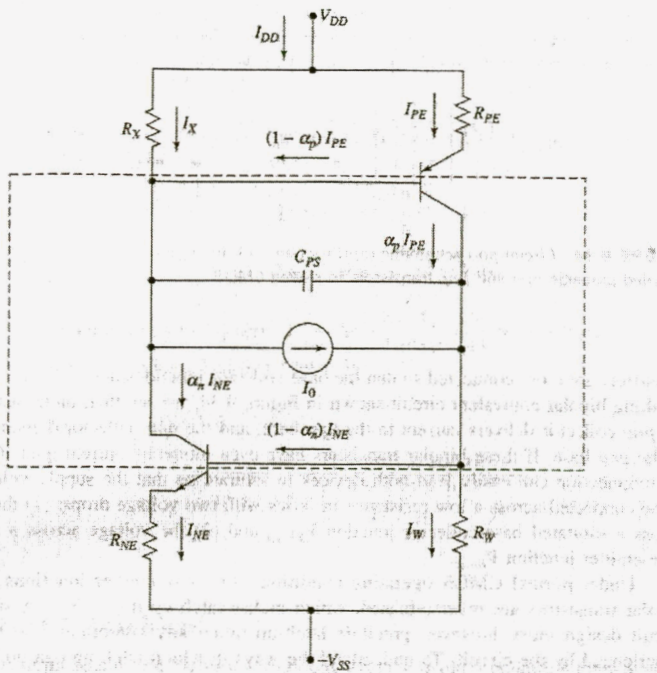


Figure 13: Latch-up equivalent circuit including well-to -substrate capacitor  $C_{PS}$  and parasitic current source  $I_0$ . The dashed lines surround all elements connected between the well and substrate nodes<sup>[3]</sup>

A Single-Event Effect (SEE) occurs via the transient current-spike caused by a heavy-ion impact. In the case of SEL, a transient current spike can turn on the base of either parasitic transistor embedded in the thyristor structure. In normal operation, the current source of Figure 3 is typically low in magnitude, and the possibility of latch-up is virtually non-existent. In space, a transient current spike increases  $I_0$  (from Figure 13), and activates the thyristor. A low-impedance current path from the power supply to ground flows, effectively shorting out the device. Once high currents flow, the device often fails. Silicon-on-insulator SEL response is quite simple; in SOI, adjacent device isolation eliminates the possibility of latch-up entirely. Elimination of latch-up is one of the primary reasons why SOI was originally adopted by the aerospace and military industries.

#### 4.1.2 Basic Mechanisms of Single-Event Upsets (SEU)

Single-Event Upsets, or 'soft errors,' can be defined as "the change of state of a bistable element caused by the impact of an energetic heavy ion or proton" within a device<sup>[13]</sup>. The particle entry results, either directly or indirectly, in the generation of electron-hole pairs in or near a reverse-biased depletion region, which then manifests into a current spike in the device. If the current spike is sufficient in magnitude, it can cause the state of a memory cell or logic storage element to change states.

Soft errors are non-destructive to the device, but can cause catastrophic system-level failures when the device is used in a critical application. Often, the affected element can be corrected by resetting or reprogramming the device. Just as a bullet fired into the ground loses energy as it travels through the layers of soil, a high energy particle



slowly loses energy as it passes through an impacted device. As the particle traverses the device, it leaves behind an energetic, electron-hole plasma track, often referred to as a ‘funnel.’ The density,  $\text{mg}/\text{cm}^3$ , of the impacted material normalizes the particle energy loss-per-unit-path,  $\text{MeV}/\text{cm}$ , resulting in a Linear Energy Transfer,  $dE/dx$ , expressed in units of  $\text{MeV}\cdot\text{cm}^2/\text{mg}$ <sup>[14]</sup>. Given a target material and value for the Linear Energy Transfer (LET) of a particle strike, one can calculate the charge deposition from the event as

$$\frac{dN}{dx} = \frac{dP}{dx} = \text{LET} * \left( \frac{mv}{w} \right) \quad (12)$$

where  $mv$  is the target-material density and  $w$  is the energy required to generate an electron-hole pair in the target material<sup>[2]</sup>.

Two common terms associated with SEUs are the LET threshold and cross-sectional area. The LET threshold is the minimum LET required to facilitate an upset in a device. The cross-sectional area represents the amount of device area sensitive to particle strikes, and decreases with device size. Specifically, the cross-sectional area is the ratio of the number of device upsets to the particle flux over a particular device surface area<sup>[12]</sup>.

The charge left behind by a particle strike knocks the impacted device out of steady state, and deposited charge moves throughout the device in one or a combination of the three basic charge transport mechanisms: drift, diffusion, and recombination. This effect can be seen by the fundamental current continuity equations

$$\frac{dn}{dt} = \frac{1}{q} \nabla \cdot (\overrightarrow{J_{ndrift}} + \overrightarrow{J_{ndiff}}) - R \quad (13)$$

and

$$\frac{dp}{dt} = \frac{1}{q} \nabla \cdot (\overrightarrow{J_{pdrift}} + \overrightarrow{J_{pdiff}}) - R, \quad (14)$$

where  $\overrightarrow{J_{ndrift}}$ ,  $\overrightarrow{J_{ndiff}}$  and  $R$  are the drift-and-diffusion current densities, and net recombination rate, respectively.

The location of impact in the device, device design and device operating conditions dictate how the generated charge moves throughout the device. Typically, the most sensitive section of a device to particle strikes is the reverse-biased pn junction. The field present in the junction immediately acts on the generated pairs, their drift results in a transient, “prompt” current within picoseconds (Figure 14). A second, delayed current component ( $Q_{DF}$  in the figure) results as carriers “generated beyond the depletion region can diffuse back toward the junction<sup>[14]</sup>.” The diffusion component is not insignificant and can last as long as hundreds of nanoseconds.

## COSMIC RAY INDUCED CURRENT PULSE

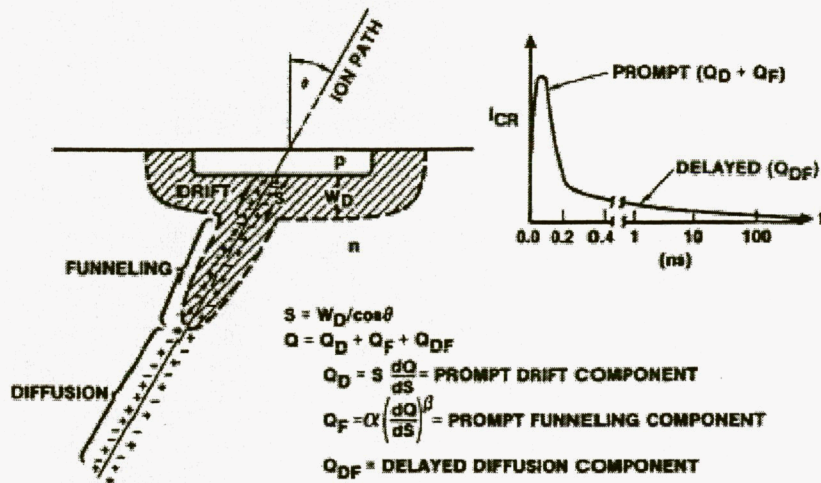


Figure 14: Cosmic ray induced current pulse showing prompt components due to drift from the depletion region and charge funneling and the delayed component due to diffusion<sup>[15]</sup>.

### 4.1.3 SOI Response to SEUs

The SOI buried oxide splits the impacting particle's ionization track into two isolated sections, as shown in Figure 15b. Whereas the bulk junction could collect charge from the entire ionization track, the only direct charge seen by the SOI junction is the thinner upper section. Figure 16 reinforces the intuitive conclusion that the cross-sectional area of an SOI device will be lower than for a bulk device of the same generation. Given the typical thickness of 100nm for a rad-hard SOI silicon film and 10um for the bulk ionization track length, the ratio of the two values gives a theoretical, SEU-sensitivity reduction of 100 by using the SOI device<sup>[13]</sup>. However, the reality is not as simple, or optimistic.



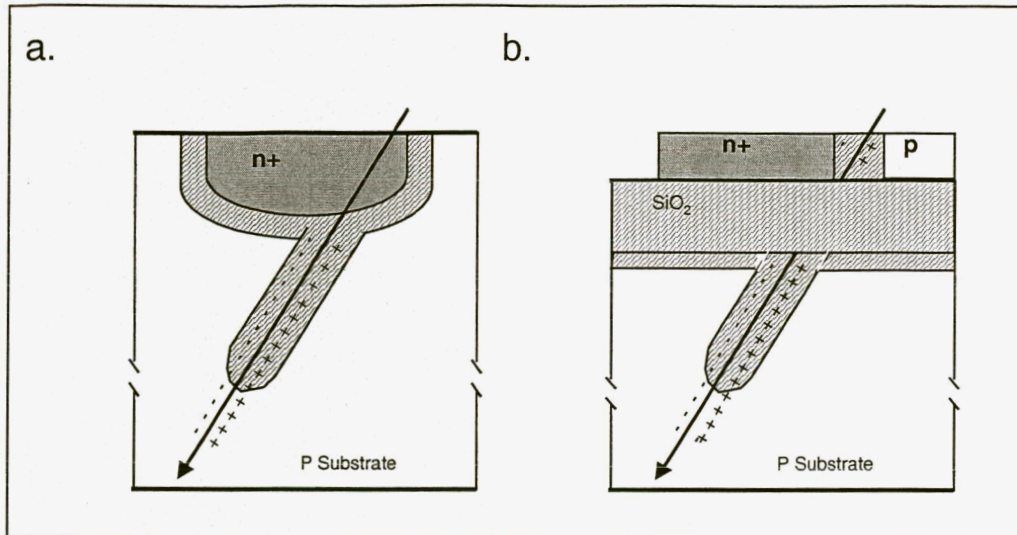


Figure 15: Conceptual distribution of charge funnels in bulk (a) and SOI (a) devices. The SOI device dramatically reduces the area for collected charge<sup>[via 2]</sup>.

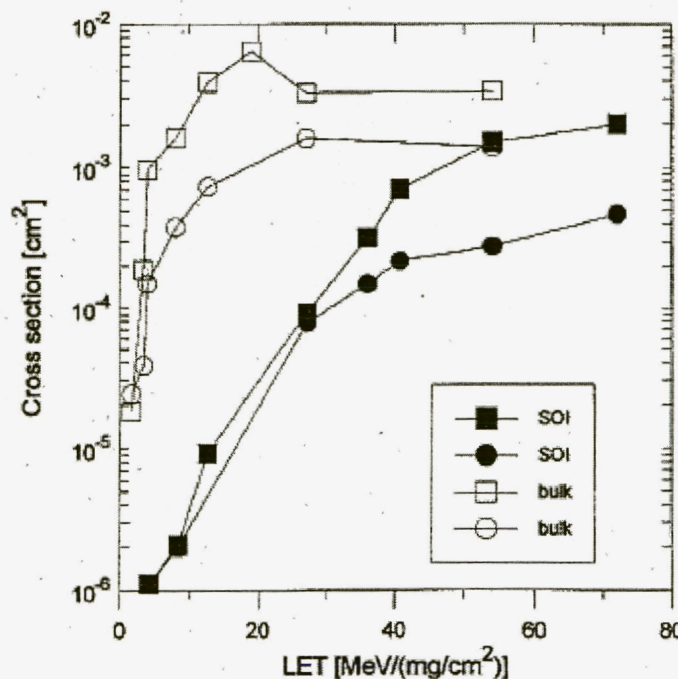


Figure 16: Sensitivity of the 68020 microprocessor, in CMOS/thick SOI and CMOS/epi technologies, for two different test programs<sup>[16 via 17]</sup>.

As previously discussed, heavy-ion strikes can generate carriers in the body of a PDSOI transistor. While the minority carriers recombine quickly, the majority carriers do not, and the floating-body potential rises. This rise in potential can easily activate the parasitic BJT structure, and the bipolar-amplified current adds to the drift current from the particle strike. In the case of PDSOI devices lacking body ties, the BJT effect on single-event transient currents can completely null the theoretical SEE sensitivity reduction mentioned above<sup>[13]</sup>. Table I shows threshold LET and BJT gain factors for

various SOI technologies. The effect of bipolar gain on SOI behavior is alleviated, but not eliminated, by the use of body ties.

Table I: Experimental and Calculated LET Threshold in SOI SRAMs in MeV/(mg/cm<sup>2</sup>), Bipolar Amplification Factors  $\beta^*$ <sup>[17]</sup>

	Experimental LET	Calculated LET	$\beta^*$
$L=1.2\ \mu\text{m}, t_{\text{Si}}=0.15\ \mu\text{m}$	46	39	0.48
$L=0.5\ \mu\text{m}, t_{\text{Si}}=0.15\ \mu\text{m}$	<15	7	2.0
$L=1.4\ \mu\text{m}$ (body ties) $t_{\text{Si}}=0.15\ \mu\text{m}$	90	117	0.28
$L=0.7\ \mu\text{m}$ (body ties) $t_{\text{Si}}=0.15\ \mu\text{m}$	52	49	0.60
$L=0.8\ \mu\text{m}, t_{\text{Si}}=1.2\ \mu\text{m}$	17	10	0.7

Figure 17 succinctly illustrates both the charge collection and bipolar amplification theories associated with SOI technology. In the bulk case, the decrease in cross-sectional area with device generation shows obvious improvements in collected charge at the struck node. However, for the SOI case, the struck-node results are skewed, for two reasons. As the SOI device geometries decrease, the relative improvement in cross sectional area is less for the SOI device as compared to bulk. Secondly, the bipolar gain of the SOI device tends to increase with reduction of gate length, explaining why the peak current for the 0.13  $\mu\text{m}$  case can be worse than for the 0.25  $\mu\text{m}$  generation<sup>[18]</sup>.

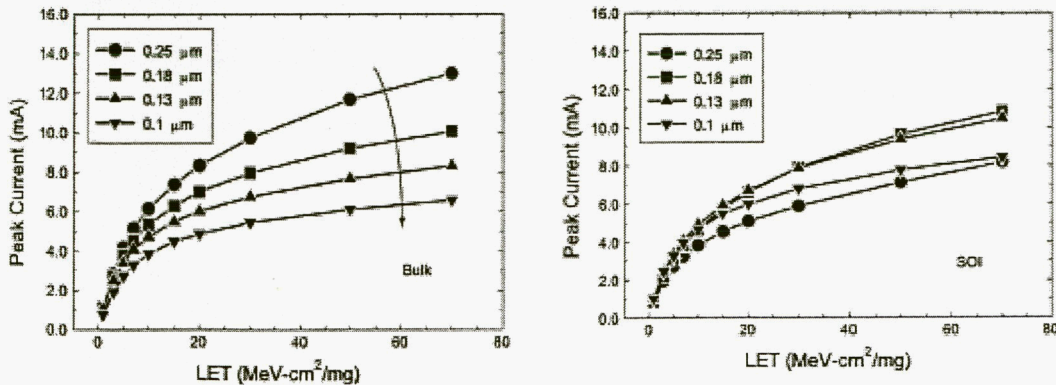


Figure 17: Peak transient current as a function of strike LET and technology scaling for bulk and SOI technologies<sup>[18]</sup>

## 4.2 SOI and Total Ionizing Dose (TID)

### 4.2.1 TID: Basic Mechanisms

Total Ionizing Dose (TID) is the integrated process of space-radiation-induced ionization within a device over a period of time; i.e. the life of a space-flight mission. The most common unit of dose is the rad. The most deleterious effect of TID on CMOS is on insulating materials within the device. Particles that impact an oxide under the presence of an electric field (i.e. the gate oxide) generate carriers in the insulator. For gate oxides, the carriers move toward either the gate/SiO<sub>2</sub> or Si/SiO<sub>2</sub> interface. Most of



the electrons leave the oxide in picoseconds, but the leftover holes are slow to leave the oxide. Once the positively-charged holes transport out of the oxide, a fraction will become trapped at the Si/SiO<sub>2</sub> interface, either due to oxide vacancies or traps within the Si band-gap at the interface<sup>[9]</sup>.

In the case of the gate oxide, the ideally-insulating structure now contains positive charge that alters gate-voltage effectiveness. In equation (5), the threshold voltage can be defined as the amount of gate voltage necessary to create a depletion region charge,  $Q_D$ , such that any additional gate voltage engenders an inversion-layer surface charge,  $Q_S$ , in the semiconductor. In Figure 18, the oxide and interface trapped charges,  $Q_{ox}$  and  $Q_F$ , cause a shift in the flat-band potential, and hence the threshold voltage. If  $V_{FB}^0$  is the metal-semiconductor work-function difference  $\Phi_{MS}$ , the shift in flat-band voltage due to trapped charges is

$$V_{FB} = V_{FB}^0 + \Delta V_{FB} = \Phi_{MS} - \frac{Q_F}{C_{OX}} - \frac{1}{C_{OX}} \int_0^{x_{ox}} \left( \frac{x}{x_{ox}} \right) \rho_{ox}^{(x)} dx \quad (15)$$

where  $\rho_{ox}^{(x)}$  is the oxide-trapped charge density as a function of position in the oxide.

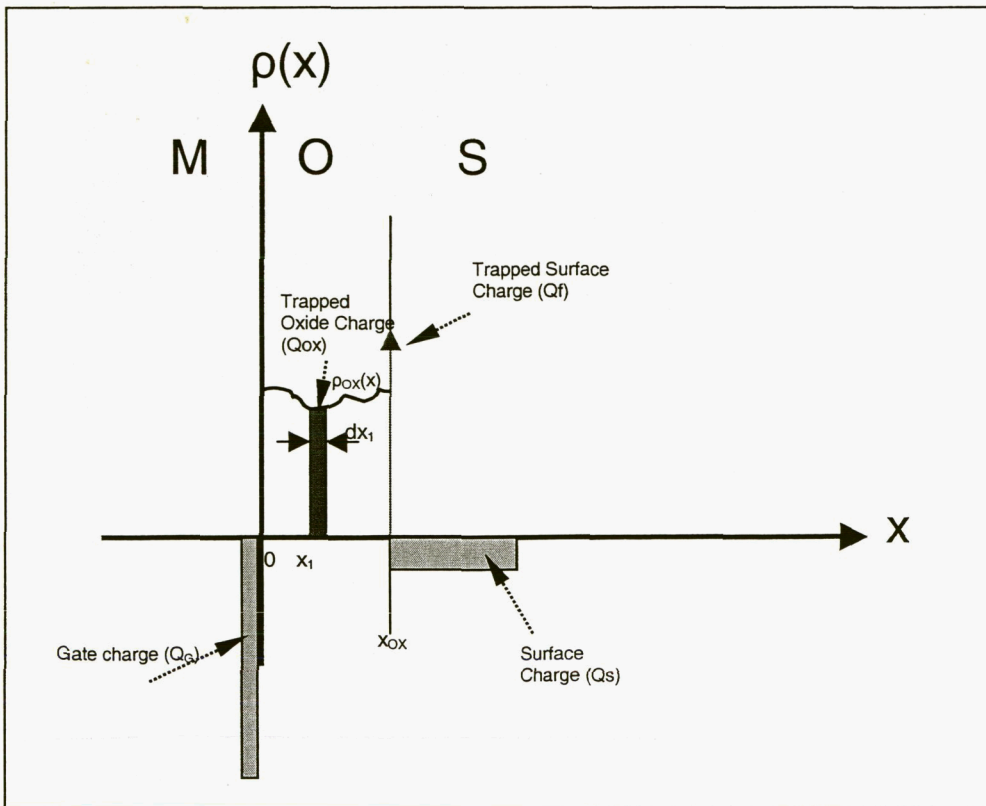


Figure 18: Trapped charge in the MOS system.

Consideration of equation (15) in terms of equation (5), one can see threshold voltage shifts are the end result for both types of traps. Oxide traps cause negative threshold voltage shifts for both n and p-type devices. Interface traps cause negative-voltage shifts for p channel, and positive shifts for n-channel, transistors<sup>[9]</sup>.

Gate threshold voltage shifts can affect both the functionality and performance of a device. Leakage-and-supply current increases, and timing failures, both result from significant deviations in the threshold voltage. If  $\Delta V_{th}$  is large enough, the gate terminal can lose control of the transistor. In a digital application, the transistor becomes frozen in either the 'ON' or 'OFF' state<sup>[12]</sup>.

Fabrication of thinner gate oxides reduces the amount of ionizing radiation in the insulator. Commercial technologies have been moving towards ultra-thin gate oxides as devices increase in speed and density<sup>[12]</sup>, thereby becoming more radiation-hard by default. However, the gate oxide is not the only insulator in MOS transistors affected by radiation. The field oxides that separate transistors in a device can also trap positive charges, resulting in a channel of electrons below the oxide. The field oxides are much thicker than the gate oxides, and often poorly fabricated with respect to trapping properties. If enough holes are trapped in the field oxide, the channel can grow wide enough to permanently connect adjacent transistors. Another effect, called edge leakage, results when trapped charges form a path for leakage current along the channel of the device. The increase in  $I_b$  under zero gate bias can be such that the device cannot be turned fully off; supply current increases, and if the power dissipation becomes high enough, the device can fail<sup>[9]</sup>.

#### 4.2.3 SOI Responses to TID

The SOI device is inherently more sensitive to TID damage than its bulk cousin. Insertion of the thick buried oxide underneath the device layer creates an increased possibility of charge traps for the SOI device. The trapped charge can affect the threshold voltage of the back-gate transistor, and increase the leakage current of the primary (front-gate) transistor. The end effect is the same as in gate oxides; leakage current increases sufficiently to disallow device control. This effect is illustrated in Figure 19.

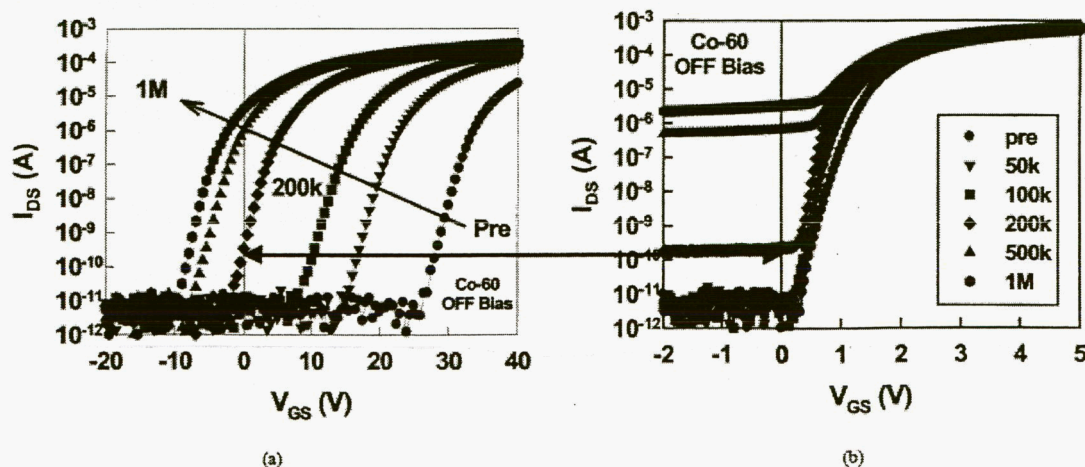


Figure 19: I-V characteristics for (a) a back-gate transistor irradiated to 1 Mrad (SiO<sub>2</sub>) and its effect on (b) the top-gate transistor leakage current. The transistors were irradiated in the OFF ( $V_{GS} = V_S = 0V$ ;  $V_{DS} = 5V$ ) bias condition<sup>[1]</sup>.

SOI total-dose hardening can be achieved using process and device design techniques to reduce the effects of trapped charge in the buried oxide<sup>[6]</sup>. A novel approach to device design was achieved in the BUSFET, developed at Sandia in 1999.



The BUSFET design disallows the PDSOI source to permeate entirely through the device layer; the impact of back-side leakage current yields significant total-dose improvements<sup>[19]</sup>. However, as device geometries shrink, even more novel approaches must be achieved to further exploit SOI's assets while minimizing its TID weaknesses<sup>[20]</sup>.

## 5.0 Conclusions

The long-standing use of silicon-on-insulator technology in military and aerospace applications originated from inherent radiation performance advantages over bulk. Recent years have found SOI utilized in Radio Frequency (RF) and high-speed microprocessors due to high-frequency, low-power characteristics, and improved processing capabilities<sup>[21][22][2]</sup>. Commercialization of SOI facilitated accelerated understanding of SOI's radiation characteristics, to the benefit of the aerospace community. The increasing use of SOI in commercial devices has the potential to yield radiation-hard, high-performance devices for future space-flight designs.

The SOI device does not come without its foibles. The floating-body and back-channel effects not only skew device behavior at placid conditions, but magnify the impact of radiation in the hostile space environment. These factors require the device designer take special precautions; particular process or design techniques often necessitate development of SOI devices to withstand harsh environments. Regardless, SOI's progress from niche toward mainstream shows no signs of reduction, and design techniques will continue to evolve as we approach Moore's barrier and beyond.

## **6.0 Personal Conclusions**

I learned an immense amount by undertaking this project. My initial topic was the study of radiation effects in devices. When I realized I had to pick a specific device, I chose SOI, as I had heard it mentioned in several occasions. At the project's inception, I had never researched anything on IEEE. At first I was overwhelmed and frustrated; I felt I may have bit off more than I could chew. As I began to fine-tune my scope, I found the PDSOI device behavior's similarity to bulk was a good basis of comparison for this fundamental discussion. I tied the background research on radiation environments and mechanisms to the PDSOI characteristics most relevant to radiation effects. As I wrote the paper, I found I had to keep removing material; the write-up could have easily doubled in length. Looking back, I feel my understanding of research and basic device behavior has accelerated by undertaking this project. All in all, I spent roughly 45 hours in development of this paper.



## References

- [1] J.R. Schwank, "Radiation Effects in SOI Technologies," IEEE Transactions on Nuclear Science, vol. 50, p. 522. June 2003.
- [2] J.P. Coligne, *Silicon on Insulator Technology: Materials to VLSI*. Boston: Kluwer, 2003.
- [3] R.S. Muller, T.I. Kamins, *Device Electronics for Integrated Circuits*. New York: John Wiley & Sons, Inc, 2003.
- [4] S.M. Sze, *Physics of Semiconductors*, 2<sup>nd</sup> Ed., J. Wiley & Sons, 1981.
- [5] "First fully depleted SOI ships from Oki Electric," <http://www.electronicweekly.com/Article28381.htm>, Feb. 2002.
- [6] K. Bernstein, *SOI Circuit Design Concepts*. Hingham, MA: Kluwer, 2000.
- [7] G.G. Shahidi, et. al, "Device and Circuit Design Issues in SOI Technology," IEEE 1998 Custom Integrated Circuits Conference, p. 339.
- [8] O. Musseau, et. al, "Laser Probing of Bipolar Amplification in 0.25- $\mu$ m MOS/SOI Transistors," IEEE Transactions on Nuclear Science, vol. 47, p.2196. December 2000.
- [9] Schwank, James R. Basic Mechanisms of Radiation Effects in the Natural Space Environment
- [10] Mazur, J.E. Space Radiation Environment. Crosslink, Summer 2003
- [11] Stassinopoulous – reference 1 in Schwank
- [12] J. Scarpulla, A. Yarbrough, "What Could Go Wrong? The Effects of Ionizing Radiation on Space Electronics," Crosslink, Summer 2003, p. 15.
- [13] A. G. Holmes-Siedle, Len Adams, *Handbook of radiation Effects*. Oxford University Press, 2002.
- [14] Dodd, Paul E. Basic Mechanisms for Single Event Effects, p. II-10
- [15] J.C. Pickel, 1983 NSREC Short Course, Gatlinburg, TN.
- [16] P. Lestrat, et. al, "SOI 68T020 Heavy Ions Evaluation," IEEE Transactions on Nuclear Science, vol. 41, p. 2240, 1994.
- [17] O. Musseau, "Single-Event Effects in SOI Technologies and Devices," IEEE Transactions on Nuclear Science, vol. 43, p. 603. April 1996.
- [18] P. Dodd, et. al, "Production and Propagation of Single-Event Transients in High-Speed Digital Logic ICs," IEEE Transactions on Nuclear Science, vol. 51, p. 3278, December 2004.
- [19] J.R. Schwank, et. al, "BUSFET: A Radiation-Hardened SOI Transistor," IEEE Transactions on Nuclear Science, vol. 46, p. 1809. December 1999.
- [20] S. Parke, "Comparison of Existing & Proposed SOI MOSFET Device Structures for Minimizing Total Dose Radiation Damage," 2004 IEEE Aerospace Conference, p. 2427.
- [21] D. Corson, P. Delatte, "Why All the Buzz about SOI?" [http://rfdesign.com/mag/radio\\_why\\_buzz\\_soi/](http://rfdesign.com/mag/radio_why_buzz_soi/), 2003.
- [22] F. Assaderaghi, G. Shahidi, "SOI at IBM: Current Status of Technology, Modeling, Design and Outlook for the 0.1 $\mu$ m Generation"